54

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/575,456	05/22/2000	James S. Cullum	M4065.0244/P244	2124

24998 7590 03/12/2003

DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L STREET NW
WASHINGTON, DC 20037-1526

EXAMINER
TRUJILLO, JAMES K

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 03/12/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/575,456	CULLUM ET AL.	
	Examiner	Art Unit	
	James K. Trujillo	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 September 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 May 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The office acknowledges the receipt of the following and placed of record in the file: Information Disclosure Statement dated 9/18/00 and Corrected Filing Receipt dated 9/27/00.

2. Claims 1-44 are presented for examination.

Drawings

3. Figures 1 and 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

4. Claim 36 is objected to because of the following informalities: line 1 of claim 36 the "s" should be "as". Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art (hereinafter AAPA) in view of Nelson et al. U.S. Patent 5,258,660 (hereinafter Nelson).

7. As to claim 1, AAPA substantially taught the invention as per claim 1 including:

a. a clock sources for supplying a first clock signal [17 figure 1];

b. a plurality of output circuits each of which receives and outputs a respective data signal, each said output circuit operating in response to a respective applied clock signal [13a-13n figure 1];

AAPA does not expressly disclose a plurality of adjustable delay circuits receiving said first clock signal, each of said adjustable delay circuits providing a respective first delayed first clock signal to a respective one of said plurality of circuits. AAPA only teaches having a single delay prior to for all respective output circuits.

Nelson substantially taught a plurality of adjustable delay circuits receiving a first clock signal, each of said adjustable delay circuits providing a respective first delayed first clock signal to a respective one of said plurality of circuits [42a-42c figure 4]. In summary, Nelson taught a system having a selected clock wherein the clock is provided to a plurality of different circuits. Clock select 32 emits a clock signal along line 34 which is then fanned out through delay circuits [skew comps] to outputs via 36. Each circuit receives a delayed clock signal that is relative to the added delay of its particular path.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify AAPA by adding adjustable delay circuits to each of the respective output circuits as taught by Nelson. Nelson suggests that delay circuits of his invention are applicable to a variety of systems necessary for precise timing control [col. 4 lines 41-46]. An artisan would have been motivated to do so because Nelson teaches it would increase the speed at which a system would run [col. 2 line 9-11].

8. As to claim 2, AAPA teaches that each of the output circuits has an associated output data hold time. As modified by Nelson as set forth hereinabove the hold times of the output circuits would be adjusted by the delay of a respective delay circuit.

9. As to claim 3, Nelson taught that the adjustable delay is programmable [col. 3 line 53 through col. 4 line 18].

10. As to claim 4, Nelson teaches that the delay of each of said adjustable delay circuits is adjusted such that the timing is substantially coincident. Nelson discloses that signals do not arrive at destination points substantially coincident (skew) due to differences in paths (without skew compensation) [col. 1 lines 29-51 and col. 2 lines 8-10]. Nelson further discloses that his invention is aimed at reducing skew (difference in times of arrival for signals) as much as possible [col. 3 lines 53-60]. In combining AAPA with Nelson as set forth hereinabove the data hold time of each output circuit would be substantially coincident because Nelson reduces the skew for signals as much as possible.

11. As to claim 5, AAPA teaches that the output circuits would be connected to data output terminals because the output circuit are used to place output to a memory device

thus requiring output terminals [page 2 lines 1-2]. Further, Nelson teaches that the delay of each of said adjustable delay circuits is adjusted such that the timing is substantially coincident. Nelson discloses that signals do not arrive at destination points substantially coincident (skew) due to differences in paths (without skew compensation) [col. 1 lines 29-51 and col. 2 lines 8-10]. Nelson further discloses that his invention is aimed at reducing skew (difference in times of arrival for signals) as much as possible [col. 3 lines 53-60]. In combining AAPA with Nelson as set forth hereinabove the data hold time of each output circuit would be substantially coincident because Nelson reduces the skew for signals as much as possible.

12. As to claim 6, as set forth hereinabove AAPA combined Nelson taught a delay circuit comprising an input for receiving said first clock signal and a plurality of delay element, each of said delay elements providing different respective delay to a signal applied thereto. The clock signal must be received and Nelson teaches that each delay element is dependent on the path of which it is a part.

Nelson further teaches an embodiment employing a switch for selectively causing a selected one of said delay elements to delay first clock signal and apply a delayed first clock signal to a respective circuit [col. 7 lines 39-65]. Wherein the multiplexers act as switches to switch in particular amounts of delay corresponding to respective paths. The multiplexers are available to switch in no delay or a maximum delay. Therefore, AAPA in combination with Nelson teach switches for switching in delay.

13. As to claim 7, Nelson taught a programming circuit for programming the switch element that selectively apply a delay to a clock signal [figures 4 and 5]. Delay select lines are used to control the delay applied to a clock signal. It is interpreted that by using the select lines the switches (multiplexers) are programmed.

14. As to claim 8, neither AAPA nor Nelson expressly discloses wherein the programming circuit comprises at least one fuse element. Nelson discloses using a multiplexer network to program and thereby switch in delay. It would have been obvious to one of ordinary skill in the art at the time of the invention to substitute fuse elements in place of the multiplexers because it is an alternative way to switch in a delay. An artisan would have been motivated to do so in an environment where space is crucial because the fuse elements require less space than the multiplexers.

15. As to claim 9, neither AAPA nor Nelson expressly discloses wherein the programming circuit comprises at least one anti-fuse element. Nelson discloses using a multiplexer network to program and thereby switch in delay. It would have been obvious to one of ordinary skill in the art at the time of the invention to substitute anti-fuse elements in place of the multiplexers because it is an alternative way to switch in a delay. An artisan would have been motivated to do so in an environment where space is crucial because the anti-fuse elements require less space than the multiplexers.

16. As to claim 10, as set forth hereinabove, the combination of AAPA and Nelson teach an apparatus wherein the switch circuit comprises a plurality of switch elements respectively coupled to said plurality of delay elements, one of said switch elements being selectively enabled to apply said first clock signal to its respectively coupled delay

element [figure 5 and col. 7 lines 39-65]. In Nelson the switch circuits contains multiplexers that switch in amounts of delay respective to the delay element.

17. As to claim 11, Nelson taught a programmable circuit for programming having switch elements that are selectively enabled [figure 5 and col. 7 lines 39-65]. Nelson uses delay select lines to program multiplexers that switch in amounts of delay.

18. As to claim 12, AAPA discloses that the output circuits are output buffer circuits [page 2 lines 11-13].

19. As to claim 13, AAPA discloses that the output circuits are applicable to be used in memory devices [page 2 lines 4-16].

20. As to claim 14, Nelson discloses, as set forth herein above, switch circuits comprising at least one multiplexer [figure 5].

21. As to claims 15-28, AAPA combined with Nelson as set forth hereinabove substantially taught the claimed data output apparatus. Therefore, together they teach the claimed processor based system.

22. As to claims 29-40, AAPA combined with Nelson as set forth hereinabove substantially taught the claimed data output apparatus. Therefore, together they teach the memory device.

23. As to claims 41-48, As to claims 15-28, AAPA combined with Nelson as set forth hereinabove substantially taught the claimed data output apparatus. Therefore, together they teach the claimed method of providing data output signals.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Pat. No. 6,167,528 to Arcoleo. This patent taught a programmable skew buffer for optimizing the timing at the input or output of a memory device.

U.S. Pat. No. 6,477,659 to Ho. This patent taught measuring timing margins between functional units using programmable delay elements.

U.S. Pat. No. 5,852,640 to Kliza et al. This patent taught a system that adaptively adjusts delay for a path of a clock.

U.S. Pat. No. 5,692,165 to Jeddeloh et al. This patent taught a system having programmable delay between a clock and an output buffer.

Hiroki Sutoh, Kimihiro Yamakoshi and Masajuk Ino, "Circuit Technique for Skew-Free Clock Distribution", IEEE, 1995, Custom Integrated Circuits Conference, 0-7803-2584-2/95, pp. 163-166. This paper teaches clock distribution techniques having automatic skew-compensation.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James K. Trujillo whose telephone number is (703) 308-6291. The examiner can normally be reached on M-F (7:30 am - 5:00 pm) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on (703) 305-9717. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

James Trujillo
March 5, 2003

THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100